Amendments to the Claims

1. (Currently Amended) An electrostatic discharge (ESD) protection circuit comprising:

an NMOS transistor connected between an input/output pad and a ground, the NMOS transistor having a parasitic bipolar transistor; and

at least one diode among a plurality of N diodes, connected between the input/output pad and the NMOS transistor, a cathode of said at least one diode being connected to the ground,

wherein, p+ and n+ junctions of a first diode of the plurality of N diodes are connected to the input/output pad and a p+ junction of a second diode of the plurality of N diodes, respectively,

the second diode through the N-1 diode of the plurality of N diodes are connected such that an n+ junction of each of the second diode through the N-1 diode is connected to the p+ junction of a subsequent diode, and

an n+ junction of an N diode is connected to the substrate.

2. (Currently Amended) The ESD protection circuit of claim 1, wherein an output terminal of the at least one diode among a plurality of N the diodes is connected to a base of the parasitic bipolar transistor.

3. (Currently Amended) The ESD protection circuit of claim 1, wherein ~~the said at least one~~ diode is a PN diode.

4. (Canceled)

5. (Currently Amended) The ESD protection circuit of claim 1, wherein ~~the at least one diode includes a plurality of N diodes, and~~

a count of the diodes N of the plurality of N diodes is determined so as to stop a current flow through the at least one diode during a normal operation of a chip.

6. (Currently Amended) The ESD protection circuit of claim ~~1~~[[4]], wherein, the plurality of N diodes are connected in series to each other in a forward direction.

7. (Canceled)

8. (Currently Amended) An electrostatic discharge (ESD) protection circuit comprising:

an input/output pad;

a plurality of N diodes connected in series between the input/output pad and a substrate of an NMOS transistor; and

the NMOS transistor is connected between the input/output pad and has a parasitic bipolar transistor connected to the plurality of N diodes, the cathode of at least one of said plurality of N diodes being connected to a ground,

wherein p+ and n+ junctions of a first diode of the plurality of N diodes are connected to the input/output pad and a p+ junction of a second diode of the plurality of N diodes, respectively,

the second diode through the N-1 diodes of the plurality of N diodes are connected such that an n+ junction of each of the second diode through the N-1 diode is connected to the p+ junction of a subsequent diode; and

an n+ junction of an N diode is connected to the substrate.

9. (Previously Presented) The ESD protection circuit of claim 8, wherein the substrate is a p-type substrate and connected to said ground.

10. (Original) The ESD protection circuit of claim 8, wherein the plurality of N diodes are PN diodes.

11. (Original) The ESD protection circuit of claim 8, wherein a number of N diodes in the plurality of N diodes is determined so as to stop a current flow through the plurality of N diodes during a normal operation of a chip.

12. (Canceled)

13. (Original) The ESD protection circuit of claim 8, wherein the output terminal from the Nth diode of the plurality of N diodes is connected to the base of the parasitic bipolar transistor.

Claims 14-18 (Canceled)